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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,754	01/26/2004	Adrian Stoica	NPO-20535-2-CU	7312

7590 07/21/2006

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NASA Management Office-JPL
4800 Oak Grove Dr.
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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)	
10/768,754	STOICA ET AL.	
Examiner	**Art Unit**	
Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/26, 5/27.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. *Claims 1-20 have been presented for examination based on applicant's disclosure filed 26 January 2004. Claims 1-20 stand rejected by the examiner.*

Drawings

2. *The drawings filed 21 October 2004 are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the must be shown or the features canceled from the claims. No new matter should be entered.*

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

MPEP Section 608.02(d) [R-2] "Complete Illustration in Drawings" recites the following:

"37 CFR 1.83. Content of drawing.
*(a) The drawing in a nonprovisional application must show **every feature** of the invention **specified in the claims**. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation"*

In this case, none of the drawings (Figs. 1-5) appear to explicitly show the claimed elements or features relating to "reconfigurable switches connected to form a

series-connected succession", or a connection at a "first power terminal of one transistor and second power terminal of the other transistor of the pair", as recited in independent claims 1, 13, and 16, or the "individual interruptable terminal-to-terminal connection" as recited in independent claim 10.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9 of U.S. Patent No. 6,728,666. *Although the conflicting claims are not identical, they are not patentably distinct from each other because:*

Claims 1-20 include limitations relating to a first and second transistor terminal, and reconfigurable switches providing terminal-to-terminal transistor connections that are series connected to successive transistor terminals all of which appear as a subset of the limitations claimed in claims 1-9 of US Patent 6,728,666.

4. Claims 1-20 are also rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent No. 6,526,556. *Although the conflicting claims are not identical, they are not patentably distinct from each other because:*

Claims 1-20 include limitations relating to a first and second transistor terminal, and reconfigurable switches providing terminal-to-terminal transistor connections that are series connected to successive transistor terminals all of which appear as a subset of the limitations claimed in claims 1-35 of US Patent 6,526,556.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 12, 14, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Specifically, the terms "nearly the same" and "about the same" in claims 12, 14, and 18 are relative terms which render the claim indefinite. The term "nearly the same" and "about the same" are not defined by the claim, the specification

does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. ***Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,378,122 issued to Levi in view of U.S. Patent 5,258,947 issued to Sourgen in further view of "A New Research Tool for Intrinsic Hardware Evolution", P. Layzell, ICSE98, 1998 (Of Record).***

Regarding independent claims 1, 10, 13, and 16: Levi teaches a genetic algorithm used for the creation of ***evolvable circuits*** *where programmable logic devices are* ***reconfigured*** *to create new designs through the use of* ***chromosomes*** *that*

*store the genetic code of the **circuit** design. (Abstract, Summary of Invention, Figs. 1-9, CL4-L7-50, CL4-L63-CL5-L65, CL8-L46-CL9-L42)*

*Levi does not explicitly teach a device (circuit) that includes a programmable mixed analog and digital circuit realized by **transistors** with **coupled source/sink terminals**.*

*Sourgen teaches a programmable (reconfigurable) circuit that is realized using plurality of **transistors having terminals coupled** via **source/sink terminals** and a plurality of **reconfigurable switches**. (Abstract, Summary of Invention, Fig. 3, CL5-L5-64, CL6-L7-65,)*

*Levi further does not explicitly teach a programmable circuit array that allows the connection of <u>any</u> **transistor terminal** to <u>any other</u> **transistor terminal**.*

*Layzell teaches the technique of providing a switch array (cross point) in conjunction with a plurality of **transistors** such that the cross point (re-configurable) switch array allows the connection of <u>any</u> **transistor terminal** to <u>any other</u> **transistor terminal**, any transistor can easily be coupled between the **power source and sink terminals**. (Fig. 4.1, page 50, para. 2) Layzell further discloses that the **control terminals** of a **first and second transistor** can be coupled between either layers, other **power terminals**, other **control terminals**, arranged as **bypass switches**, or **together**. (Fig. 4.1, page 50, para. 2)*

*It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Levi relating to a genetic algorithm used for the creation of **evolvable circuits**, with the teaching of Sourgen*

relating to a programmable (reconfigurable) circuit that is realized using ***transistors coupled*** *via* ***source/sink terminals and reconfigurable switches,*** *and to further modify the teachings of Levi with the teachings of Layzell relating to a re-configurable switch array with* ***transistors*** *allowing coupling between the* ***power source and sink terminals*** *to realize an* ***evolvable circuit*** *incorporating* ***reconfigurable switches.*** *An obvious motivation exists since, as referenced by prior art, realizing evolving analog and digital hardware with a programmable transistor array improves the flexibility and survivability of electronic circuits. (Layzell: Abstract)*

Regarding dependent claims 2, 11, 12, 14, 17, and 18: These claims merely require that the switches be within an order of magnitude of the number of terminals of the transistors and be "nearly the same" as the number of terminals. These limitations are rendered obvious by the combination of Levi, Sourgen, and Layzell, since the number of transistor terminals is by necessity always three (i.e. base, emitter, collector) and each switch is by design choice configured using transistor and therefor would always be within an order of magnitude (i.e. less than the next power) of the number of terminals.

Regarding dependent claims 3, 15, and 20: These claims merely require that the reconfigurable switches have variable conductance. The examiner notes that this feature would be by necessity be part of any switch realized using transistors since it is well established in MOSFET devices, the conductance of the device increases linearly with the applied gate voltage (i.e. is a variable conductance).

Regarding dependent claims 4-9, and 19: These claims include limitations relating to the addition of a second, third, forth, and fifth plurality of reconfigurable switches. Here applicants appear to have merely claimed a duplicate reconfigurable switches and plural respective series-connected successions of transistors.

MPEP 2144.04 recites the following:

> *"B. Duplication of Parts*
> *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Claims at issue were directed to a water-tight masonry structure wherein a water seal of flexible material fills the joints which form between adjacent pours of concrete. The claimed water seal has a "web" which lies ** in the joint, and a plurality of "ribs" ** >projecting outwardly from each side of the web into one of the adjacent concrete slabs. <The prior art disclosed a flexible water stop for preventing passage of water between masses of concrete in the shape of a plus sign (+). Although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.)."*

The examiner therefor submits that the recited second, third, forth, and fifth plurality of reconfigurable switches are rendered obvious by the evolvable circuit combination of Levi, Sourgen, and Layzell and appear to be a mere duplication of parts since there is no claimed operational significance between the two.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,363,519 issued to Levi et al teaches evolving hardware

U.S. Patent 6,363,517 issued to Levi et al teaches evolving hardware

U.S. Patent 5,970,487 issued to Shackleford et al teaches evolving hardware

U.S. Patent 5,677,691 issued to Hosticka et al teaches configurable analog and digital array

U.S. Patent 5,021,856 issued to Wheaton teaches programmable transistor cell

U.S. Patent 6,360,191 issued to Koza teaches automatic design using genetic programming

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached at 571-272-2279. The Official Fax Number is: (703) 872-9306

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June 5, 2006

Fred Ferris
Primary Examiner

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NPO-20535-2-CU Serial No.: To be Assigned

Applicant(s): Adrian STOICA, et al.

Filing Date: Herewith Group: Unknown

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

U. S. PATENTS

Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
[illegible]	US-5,258,947	11-02-1993	SOURGEN	365	96	12-07-1990
[illegible]	US-5,677,691	10-14-07	HOSTICKA ET AL.	341	155	06-25-1993
[illegible]	US-5,705,938	01-06-1998	KEAN	326	39	09-05-1995
[illegible]	US-5,867,397	02-02-1999	KOZA ET AL.	364	489	02-20-1996
[illegible]	US-5,897,628	04-27-1999	KITANO	706	13	09-10-1996
[illegible]	US-5,959,871	09-28-1999	PIERZCHALA ET AL.	364	489	12-22-1994
[illegible]	US-5,970,487	10-19-1999	SHACKLEFORD ET AL.	707	6	08-13-1997
[illegible]	US-6,360,191	03-19-2002	KOZA ET AL.	703	6	01-05-1999
[illegible]	US-6,363,517	03-26-2002	LEVI ET AL.	716	16	06-17-1999
[illegible]	US-6,363,519	03-26-2002	LEVI ET AL.	716	16	06-17-1999
[illegible]	US-6,378,122	04-23-2002	LEVI ET AL.	716	16	06-17-1999

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
[illegible]	Augusto, Soares J.A., and Almeida, Beltran C.F., "Analog Fault Diagnosis in Nonlinear DC Circuits with an Evolutionary Algorithm," *IEEE*, July 2000, pp. 609-616.
[illegible]	Layzell, Paul, "A New Research Tool for Intrinsic Hardware Evolution," Second International Conference, *ICES98*, Lausanne, Switzerland, Springer, September 23-25, 1998, pp. 47-56.
[illegible]	

Examiner's Signature: [signature] Date Considered: 6/5/07

Initial if reference was considered, whether or not citation with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
✓	Perkowski, M. Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints," *Proceedings of the First NASA/DoD Workshop*, July 19-21, 1999, pp. 129-138.
✓	Stoica, Adrian, "Reconfigurable Transistor Arrays for Evolvable Hardware," NASA Tech Brief, Vol. 25, No. 2, Item # from JPL New Technology Report NPO-20078, July 26, 1996, pp5a.
✓	Stoica, Adrian, "Evolvable Hardware: From On-Chip Circuit Synthesis to Evolvabale Space," *IEEE*, May 2000, pp. 1-9.
✓	Stoica, Adrian, "Toward Evolvable Hardware Chips: Experiments with a Programmable Transistor Array," *IEEE*, April, 1999, pp. 1-7.
✓	Stoica, A., Keymeulen, D., Duong, V., and Salazar-Lazaro, C., "Automatic Synthesis and Fault-Tolerant Experiments on an Evolvable Hardware Platform," *IEEE*, October 2000, pp. 465-471.
✓	Stoica, A., Keymeulen, D., Salazar-Lazaro, C., Li, W., Hayworth, K., and Tawel, R., "Toward On-board Synthesis and Adaption of Electric Functions: An Evolvable Hardware Approach," *IEEE*, Vol. 2, March, 1999, pp. 351-357.
✓	Stoica, A., Keymeulen, D., Tawel, R., Salazar-Lazaro, C., and Li, W., "Evolutionary experiments with a fine-grained reconfigurable architecture for analog and digital CMOS circuits," *Evolvable Hardware '99: Proceedings of the First NASA/DoD Workshop on Evolvable Hardware*, Pasadena, CA, July 19-21, 1999.
✓	Stoica, A., Salazar-Lazaro, C., and Tawel, R., "Evolvable Electronic Systems," *1998 Military and Aerospace Applications of Programmable Devices and Technologies (MAPLD) Conference*, Pasadena, CA, September 15-16, 1998.

Examiner's Signature: [signature] Date Considered: 6/5/06

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U. S. PATENTS

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FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
2	Stoica, A., Keymeulen, D., Zebulum, R., Thakoor, A., Daud, T., Klimeck, G., Jin, Y., Tawel, R., and Duong, V., "Evolution of analog circuits on Field Programmable Transistor Arrays," *IEEE*, July, 2000, pp. 1-10.
3	Stoica, A., Klimeck, G., Salazar-Lazaro, C., Keymeulen, D., and Thakoor, A., "Evolutionary Design of Electronic Devices and Circuits," *Evolutionary Computation, Proceedings of the 1999 Congress*, Washington, D.C., July 6-9, 1999, pp. 1271-1278.
3	Zebulum, R., Pacheco, M., "Evolvable Hardware: On the Automatic Synthesis of Analog Control Systems," *IEEE*, March, 2000, pp. 451-463.
2	Zebulum, R., Stoica, A., and Keymeulen, D., "A Flexible Model of a CMOS Field Programmable Transistor Array Targeted for Hardware Evolution," *3rd International Conference of Evolvable Systems, ICES2000*, Edinburgh, Scotland, April, 2000.

Examiner's Signature: [signature] Date Considered: 6/15/06

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Sheet 1 of 2	Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU

Examiner Initials	NON PATENT LITERATURE DOCUMENTS
	BENNETT, F. III, et al. "Evolution of a 60 decibel Op Amp Using Genetic Programming", *First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 455-469.
	FLOCKTON, STUART J., et al., "Intrinsic Circuit Evolution Using Programmable Analogue Arrays," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Switzerland, 1998, pp. 144-153.
	IBA, HITISHI, et al., "Machine Learning Approach to Gate-Level Evolvable Hardware," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 327-343.
	KAJITANI, ISAMU, et al., "A gate-level Ettw Chip: Implementing GA operations and reconfigurable hardware on a single LSI," *Proc. Of the Second Int'l. Conf. On Evolvable Sytems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 1-12.
	KOZA, JOHN R., et al., "Reuse, Parameterized Reuse, and Hierarchical Reuse of Substructures in Evolving Electrical Circuits Using Genetic Programming," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 312-326.
	KOZA, JOHN R., et al., "Automated WYWIWYG Design of Both the Topology and Component Values of Electrical Circutis Using Genetic Programming," *Proc. Of the First Annual Genetic Programming Conference*, MIT Press, Cambridge MA, 1996, pp. 123-131.
	KOZA, JOHN R. et al., "Automated Synthesis of Analog Electrical Circuits by Means of Genetic Programming," *IEEE Transaction on Evolutionary Computation*, Vol. 1, No. 2, 1997, pp. 109-128.
	LOHN, JASON D., et al., "Automated Analog Circuit Synthesis Using a Linear Representation," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 125-133.
	MURAKAWA, MASAHIRO, et al., "Analogue EHW Chip for Intermediate Frequency Filters," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 143-143.
	STOICA, ADRIAN, "On Hardware Evolvability and Levels of Granularity," *International Conference On Intelligent Systems and Semiotics*, NIST, Gaithersburg VA, September 1997, pp. 244-247.
	THOMPSON, ADRIAN, "Silicon Evolution," *Proc. Of the First Annual Genetic Programming Conference*, MIT Press, Cambridge MA, 1996, pp. 444-452.
	THOMPSON, ADRIAN, "On the Automatic Design of Robust Electronics Through Artificial Evolution," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Switzerland, 1998, pp. 13-24.
	THOMPSON, ADRIAN, "An evolved circuit, intrinsic in silicon, entwined with physics," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 390-405.

Examiner's Signature: [signature] | Date Considered: 6/5/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Sheet 2 of 2	Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU

Examiner Initials	NON PATENT LITERATURE DOCUMENTS
?	ZEBULUM, RICHARD S., et al., "Evolvable Systems in Hardware Design: Taxonomy, Survey and Applications," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 344-358.
?	ZEBULUM, RICHARD S., et al., "Analog Circuits Evolution in Extrinsic and Intrinsic Modes," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 154-165.

Examiner's Signature: [signature] Date Considered: 6/5/06

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Notice of References Cited

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10/768,754	STOICA ET AL.	
Examiner	Art Unit	Page 1 of 1
Fred Ferris	2128	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,363,519	03-2002	Levi et al.	716/16
*	B	US-6,363,517	03-2002	Levi et al.	716/6
*	C	US-5,970,487	10-1999	Shackleford et al.	707/6
*	D	US-5,677,691	10-1997	Hosticka et al.	341/155
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